



Memory Technology Directions Platform 2001

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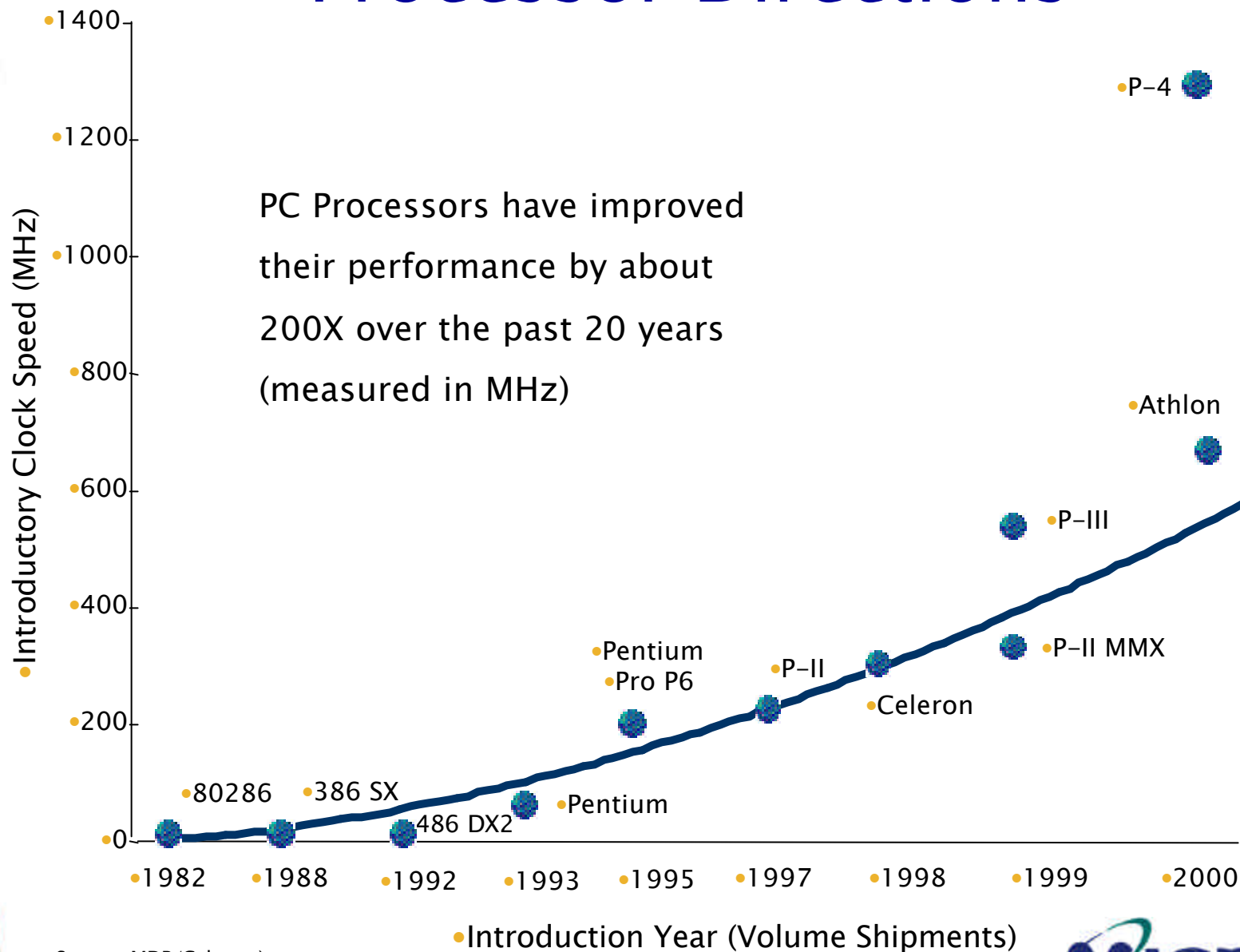


Factors Driving Memory Technology

- ❏ Processor business driven by performance
- ❏ Memory industry rewarded for integration – process for low leakage, not high speed

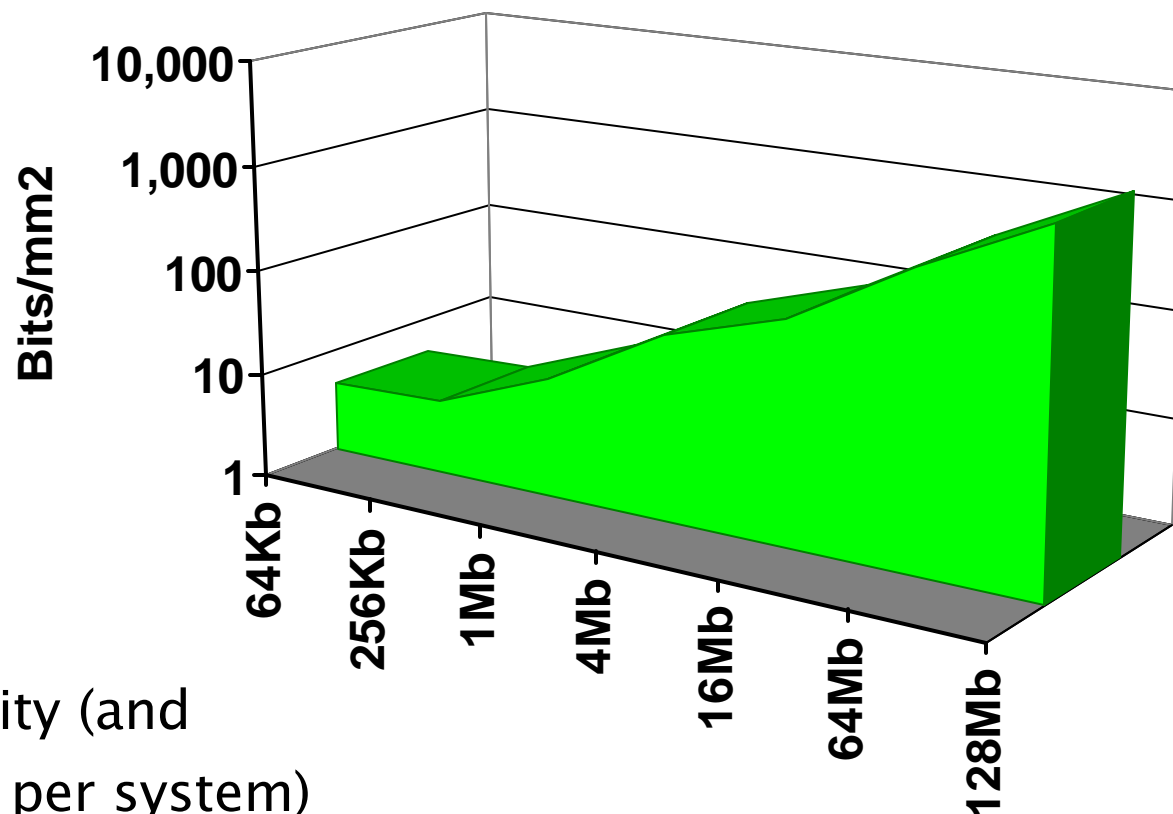


Processor Directions





Memory Directions



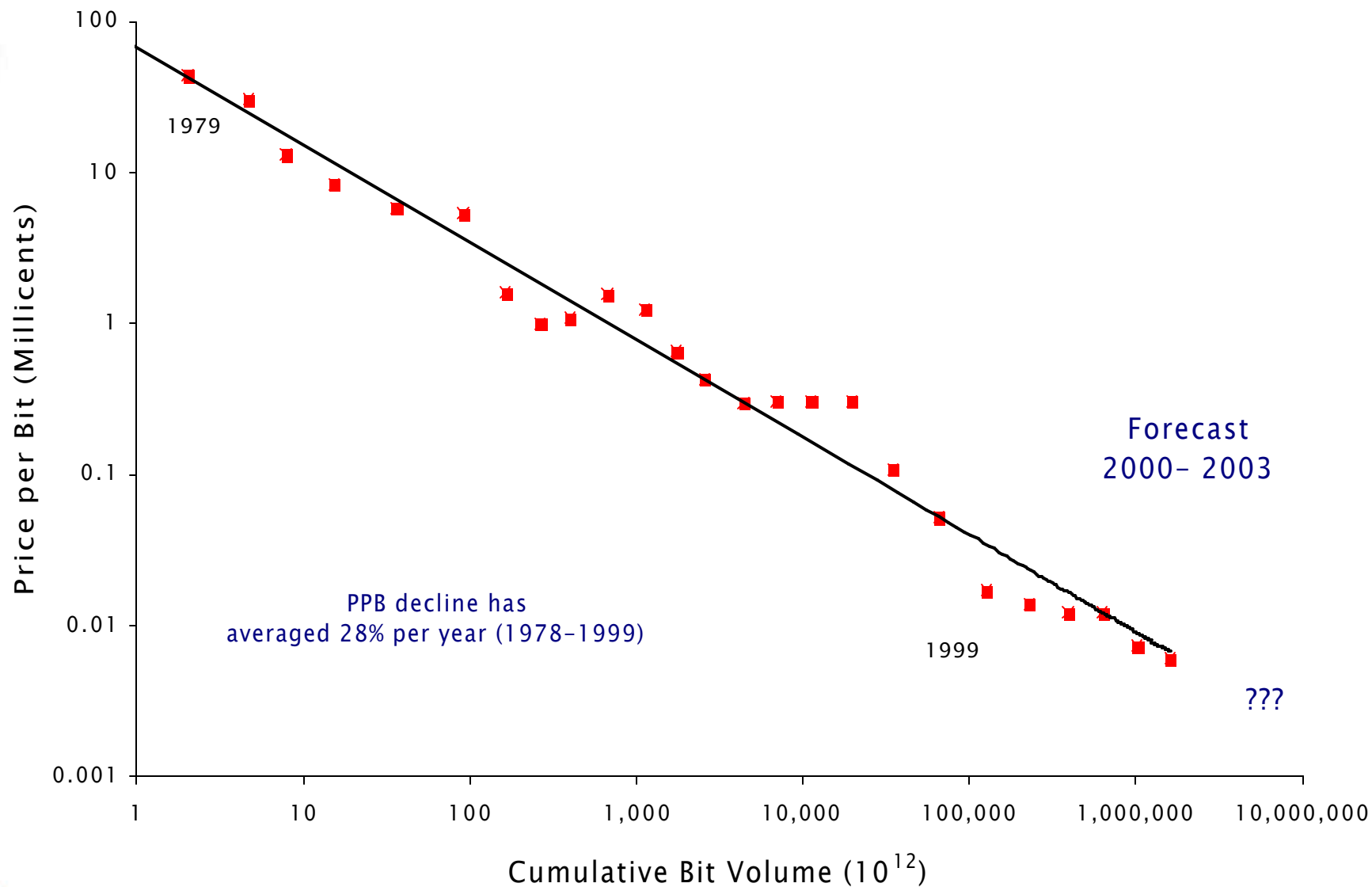
Memory bit density (and average memory per system) has increased over 2000X in the past 20 years

Source: Micron Technology, Inc.





DRAM Directions



Source: ICE Status '99 1979-1997
Semico Research 08/00, 1998-2003





Emerging Memory



DDR Development



Component

- ? All major DRAM vendors are designing and producing to the JEDEC DDR standard data sheet



Module

- ? JEDEC has defined pinout, block diagram, and SPD
- ? AMI2 is coordinating the design on standard common Gerber files for module PCB
 - 📦 184-pin unbuffered and registered DIMM Gerbers are production-ready
 - 📦 200-pin SODIMM Gerbers are ready for 1Q01 production



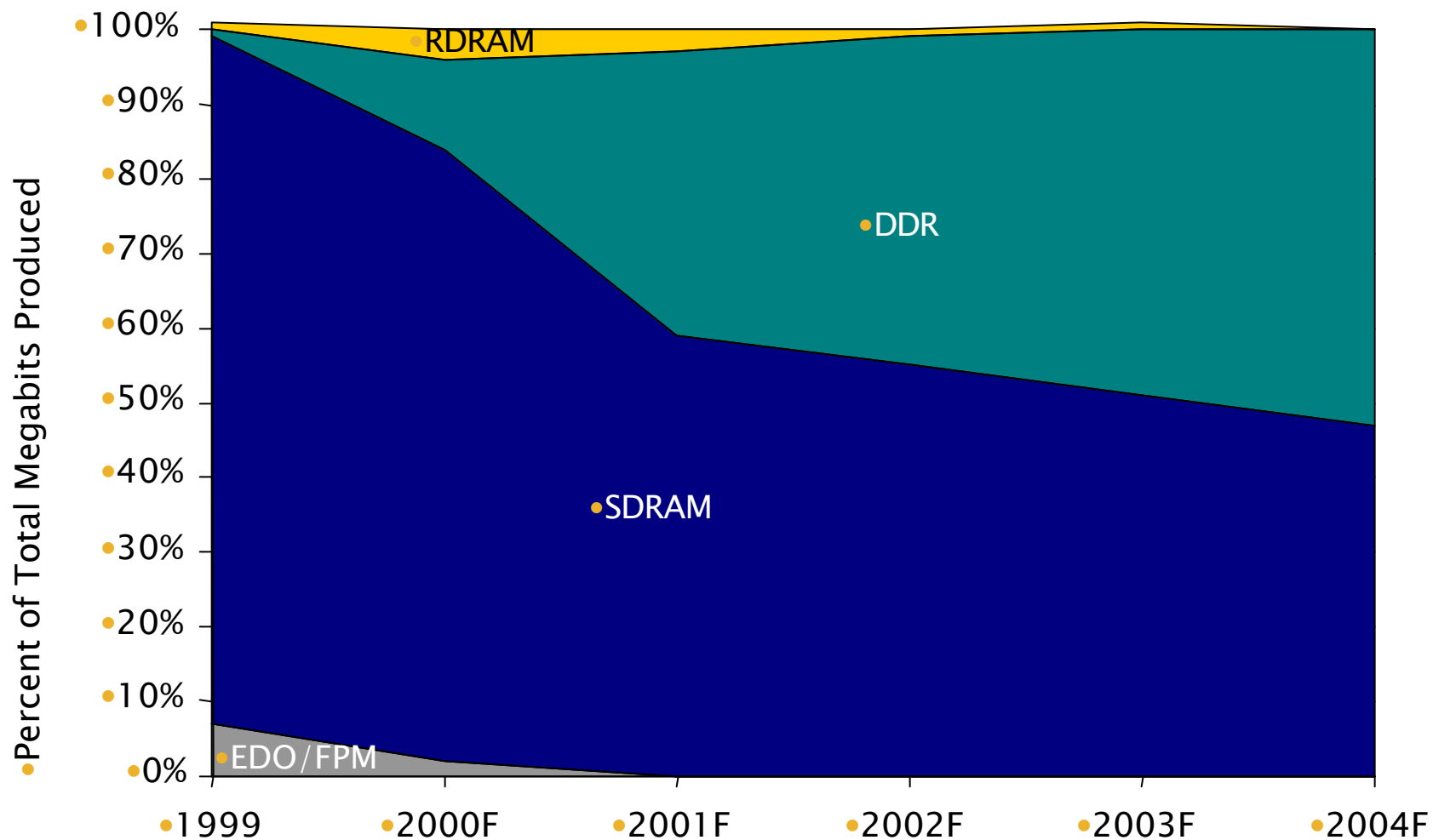
DDR SDRAM Memory Adoption

- ✦ AMD Athlon with 760 demonstrates the power of DDR
- ✦ DDR is the memory of choice for new server, workstation, and high-end desktop systems
- ✦ DDR as a point-to-point memory subsystem is the memory of choice for fixed-footprint applications





DDR Memory Adoption



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Source: Semico Research, 05/00



DDR Adoption Issues

- ✚ Misconception: DDR price delta over SDRAM
 - ✚ Some availability issues
 - ✚ Core logic solutions
 - ✚ “Correct by design” PCBs
-
- ✚ Recommendation: DO NOT try mixed DDR/SDR solutions



Future Memory Guidelines



Requirements of a Future Memory Technology

The Challenges:

- ✚ Add performance – without additional cost
 - ? No (or minimal) additional component cost
 - ? No (or minimal) additional system cost
- ✚ Solve needs of a wide range of systems
- ✚ Keep power and physical form factors in check



System in a Package (SIP)

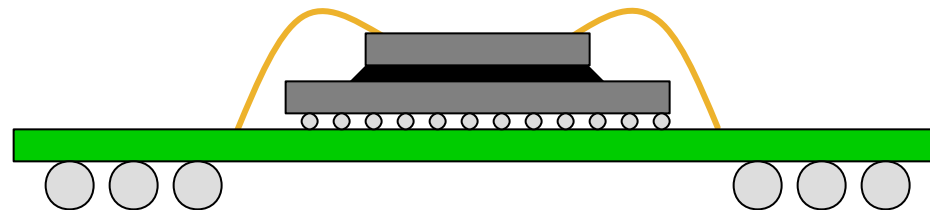
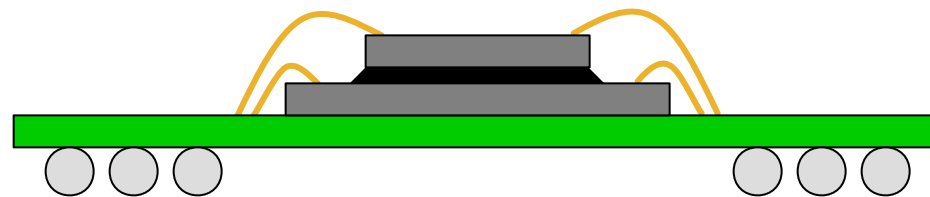


SIP Directions

- ❏ SIP allows multiple technologies in single packages: Logic, DRAM, and Flash
- ❏ Ideally, components are designed for SIP
- ❏ Required: Known Good Die (KGD)
- ❏ Benefits: reduced space, even reduced cost
- ❏ Used in portable graphics, cell phones today.



SIP Directions





Embedded Memory

- 📦 Early applications were in PC Graphics (NeoMagic)
- 📦 Today's applications:
 - ? Peripherals (printers, cameras, HDD)
 - ? Non-PC computing (WinCE, PalmOS)
 - ? L3 cache



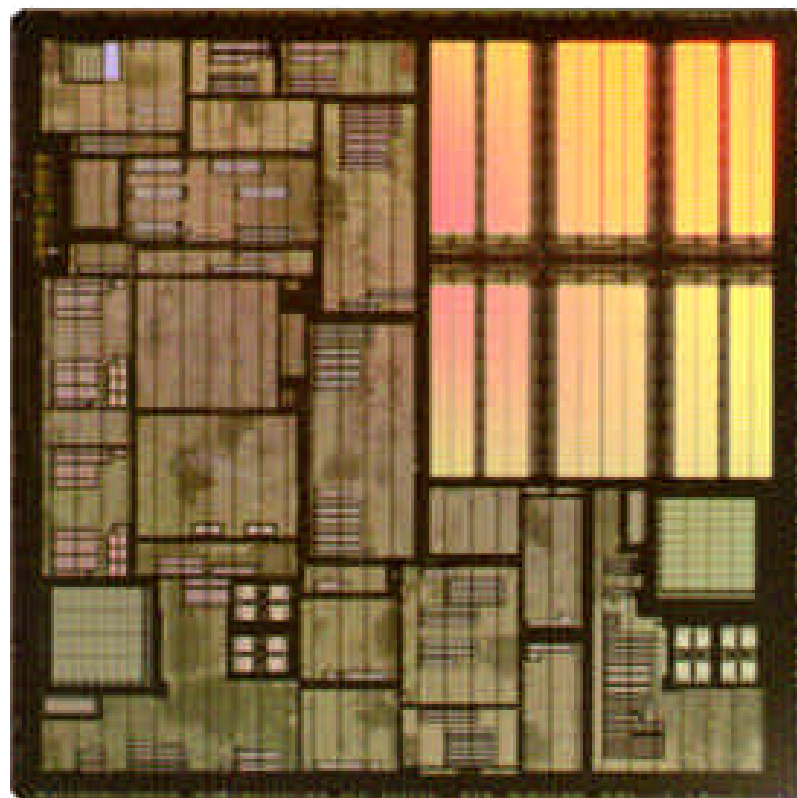


eDRAM Demonstration and Technology



Micron eDRAM: V4400e Statistics

- ✚ The NVIDIA GeForce has 23 Million transistors
- ✚ The Intel® P®-III has 28M transistors
- ✚ The Intel P-4 has 42M transistors
- ✚ **V4400: Over 125M transistors!**

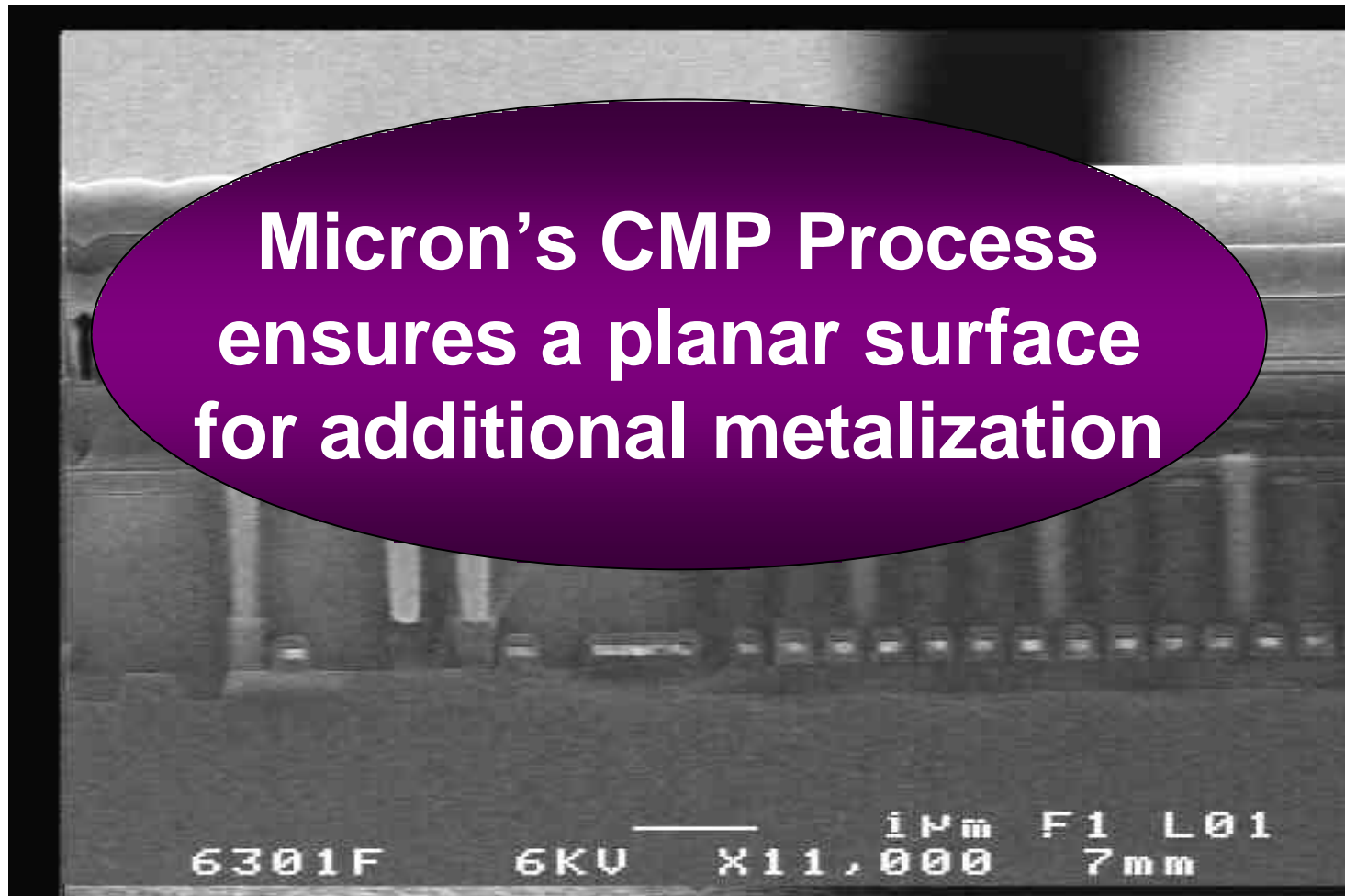


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Micron Array Edge

**Micron's CMP Process
ensures a planar surface
for additional metalization**



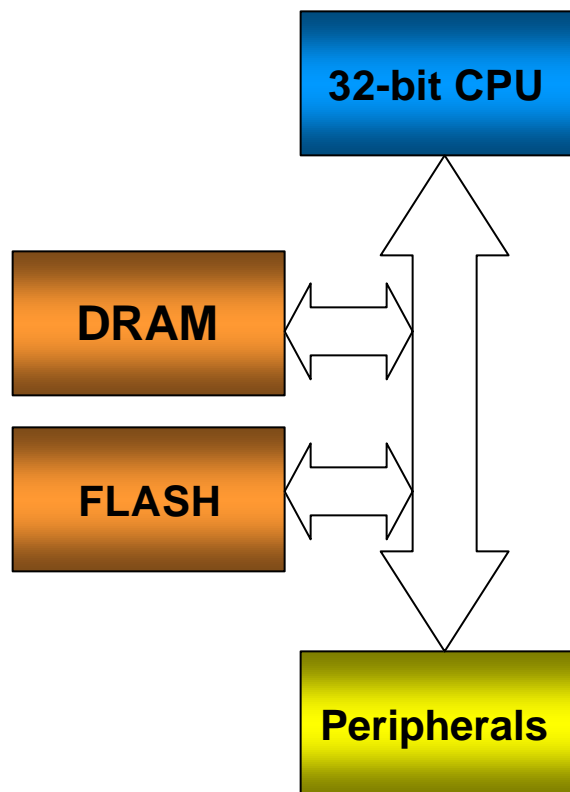


System on a Chip (S.O.C.) with eDRAM

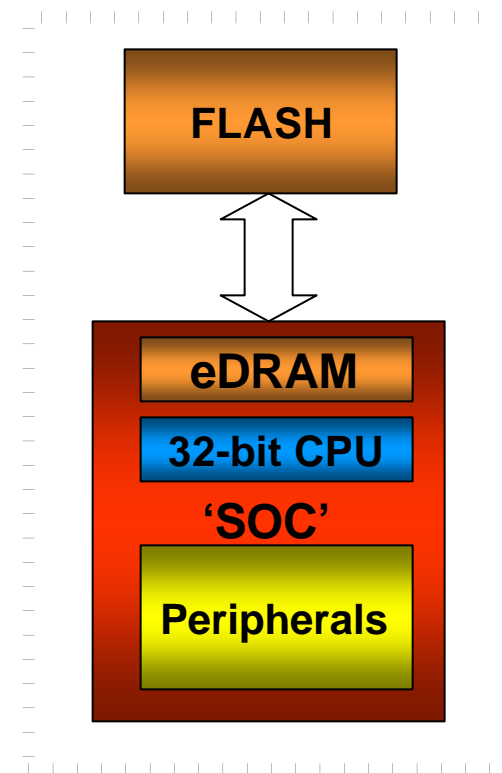


SOC: Repartitioning

 Today:



 Tomorrow:



'SIP' Solutions




eDRAM L3 Cache



Current North Bridge Component

Wasted silicon wastes money!

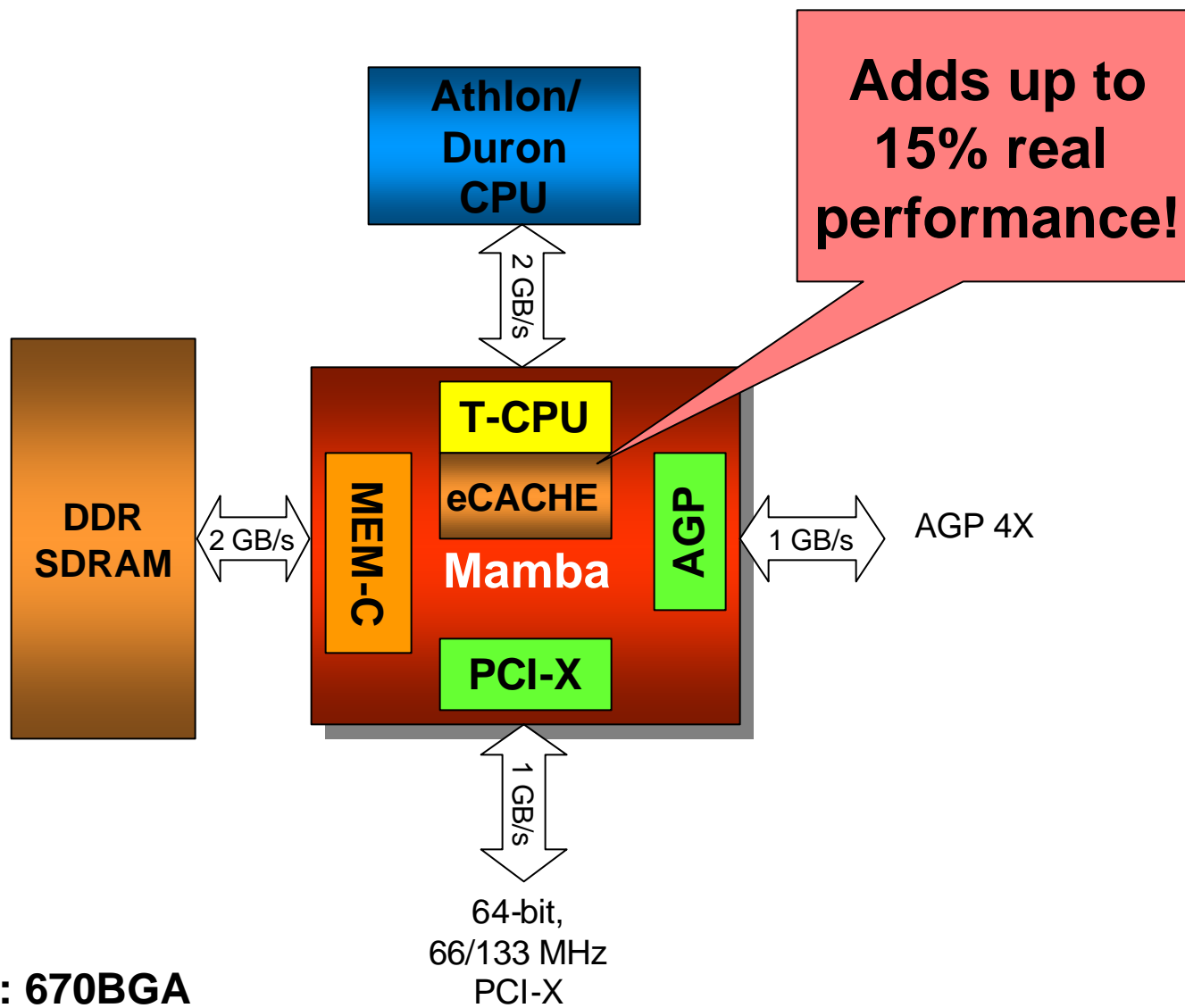


What can we do?
ECACHE!





Mamba



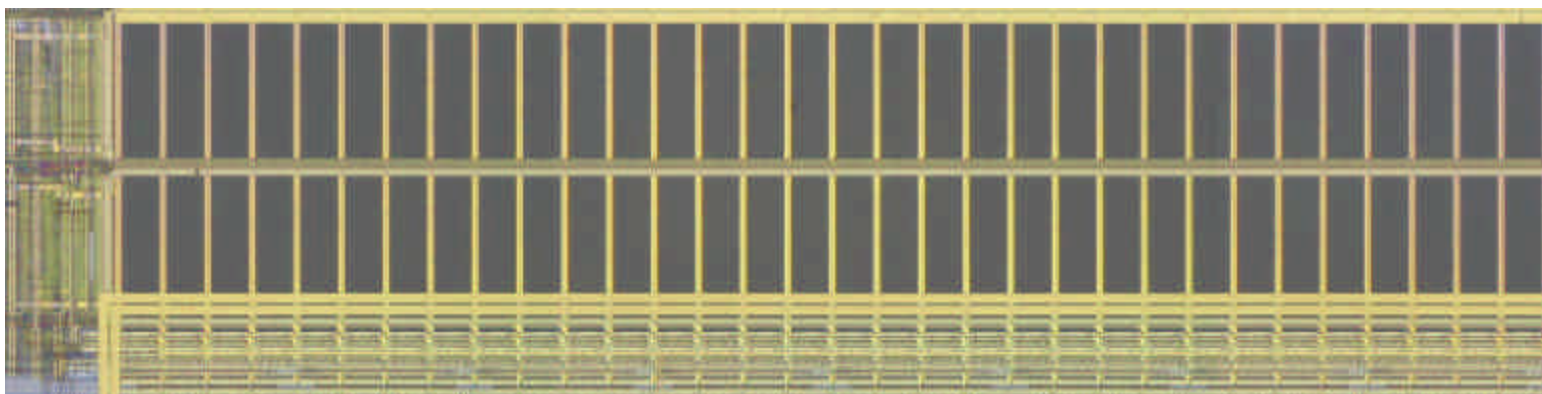
Package: 670BGA

64-bit,
66/133 MHz
PCI-X





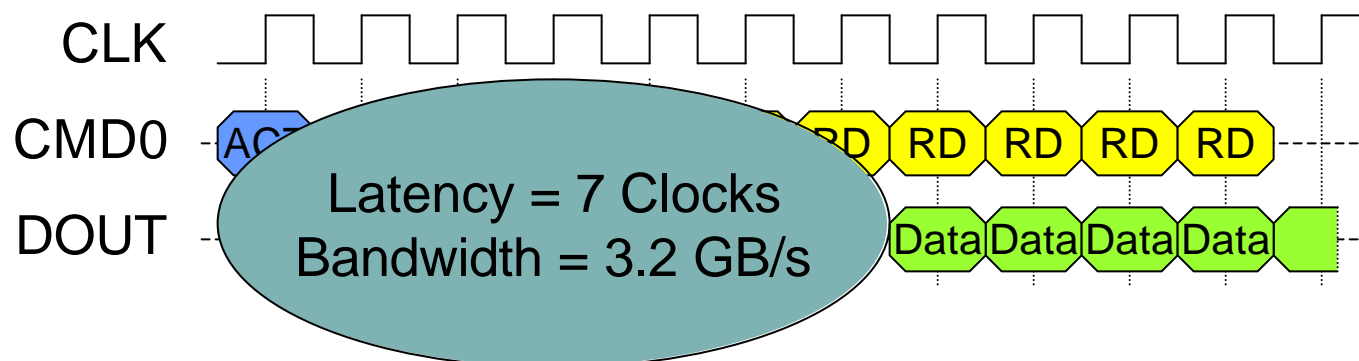
Micron's 1 MB eDRAM Core



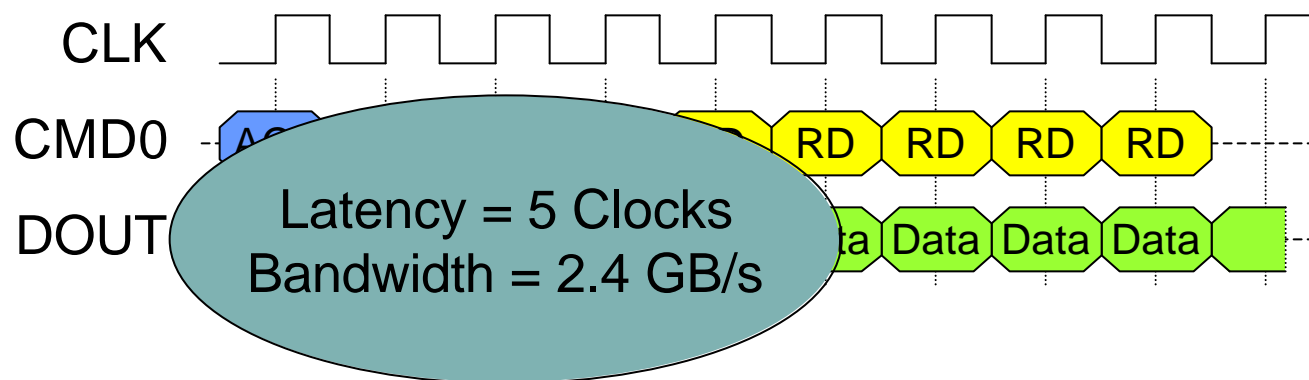


eDRAM Access

Standard eDRAM core

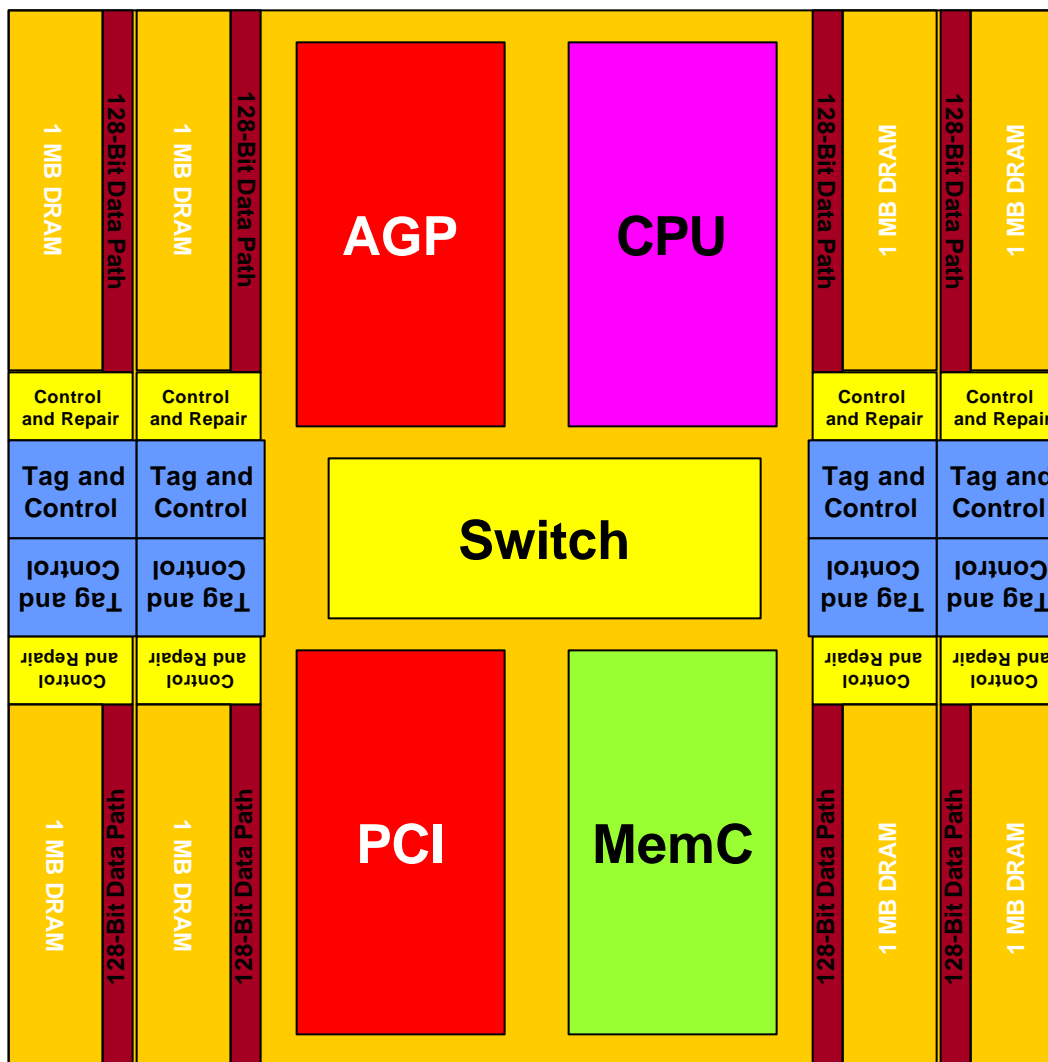


Mamba-enhanced eDRAM core





Mamba eCache



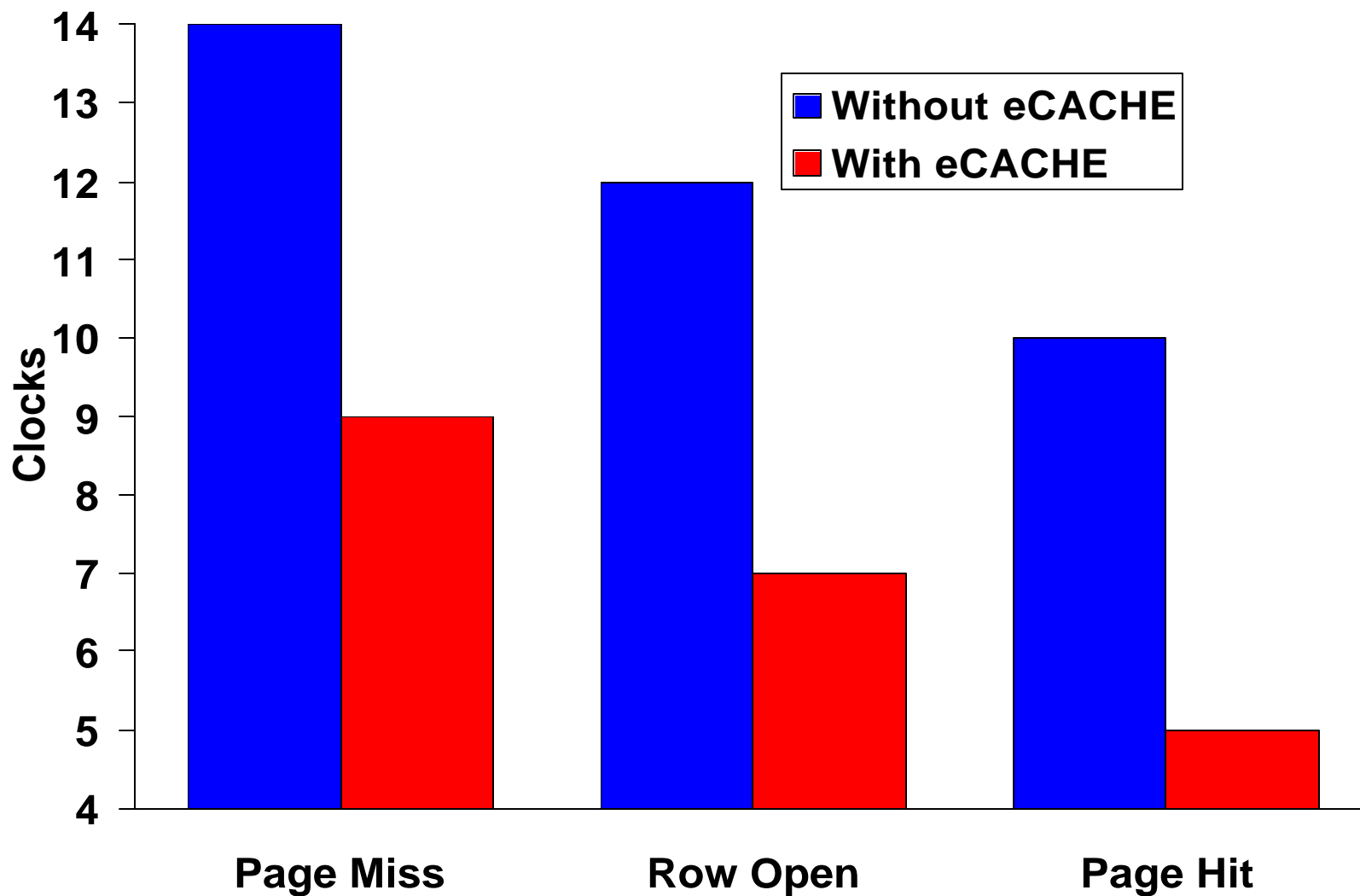


eCache Bandwidths

- ✦ eDRAM aggregate bandwidth is limited only by die size
- ✦ eCache aggregate eDRAM burst bandwidth is over 19 GB/s
- ✦ As implemented, it allows simultaneous access to four arrays and four device ports, with a sustainable bandwidth from memory of 9.6 GB/s
- ✦ Command, access, refresh, and precharge times can be overlapped, allowing sustained 9.6 GB/s



eCache Latency



(DRAM shown with 2-2-2 timing, 3-3-3 is worse)



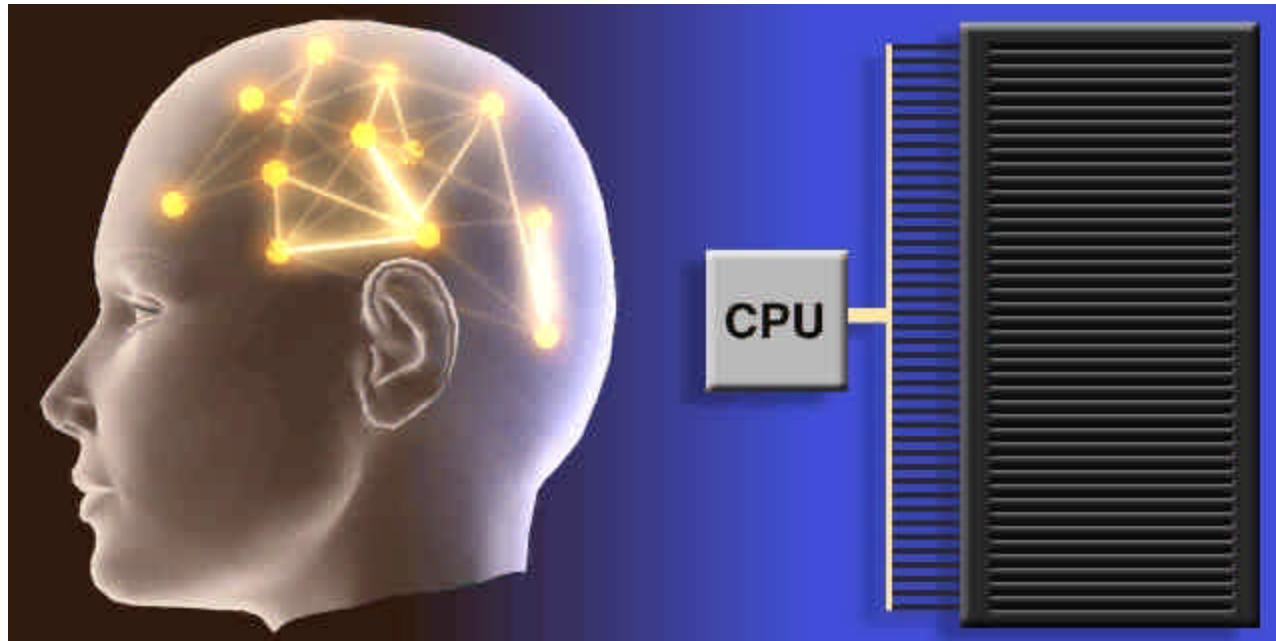


Micron eDRAM eCache

- ✦ Embedded DRAM can be built cost effectively
 - ? Can improve performance both on-chip and off chip
 - ? Granularity allows size to be tailored to fit application
- ✦ Architectural decisions made with eCache allow low latency and high bandwidth
- ✦ Core logic architecture allows maximum utilization of eCache



Future Memory? Smart Memory





Conclusions

- ✦ Different solutions for different platforms – divergence, specialization
- ✦ The industry is evolutionary – understand it!



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